ECSE 330 Assignment 2

# Introduction

The purpose of this assignment was to create a design specification for a Cascode Amplifier with respect to the boundary constraints provided by the assignment. A Cascode amplifier is a two stage amplifier as shown below –

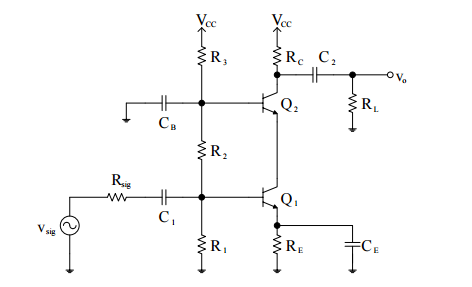


Figure : Cascode Amplifier

The outcome of this design is the determination of the values of C1, C2, CE, CB, R1, R2, R3, RC, and RE. We then proceed to simulate this circuit model in PSPICE.

# Design Constraints and Requirements

## Simulation Output Requirements

The following conditions have to be met by our design for this assignment –

* Overall gain Gv ( vo/vsig) ≥ 25 V/V
* Bandwidth (3-dB frequencies) fL ≤ 350Hz, and fH ≥ 1 MHz.
* Output voltage swing (peak-to-peak) ≥ 0.5 V
* DC power consumption ≤ 30mW

## Resources Available

* VCC = 15 V
* Rsig = RL = 1 kΩ
* One 100 μF capacitor.
* Other capacitors must be less than 5 μF.
* Available Resistors – 10 Ω, 12 Ω, 15 Ω, 18 Ω, 22 Ω, 27 Ω, 33 Ω, 39 Ω, 47 Ω, 56 Ω, 68 Ω, 82 Ω; 100 Ω, 120 Ω, 150 Ω, 180 Ω, 220 Ω, 270 Ω, 330 Ω, 390 Ω, 470 Ω, 560 Ω, 680 Ω, 820 Ω; 1 kΩ, 1.2 kΩ, 1.5 kΩ, 1.8 kΩ, 2.2 kΩ, 2.7 kΩ, 3.3 kΩ, 3.9 kΩ, 4.7 kΩ, 5.6 kΩ, 6.8 kΩ, 8.2 kΩ; 10 kΩ, 12 kΩ, 15 kΩ, 18 kΩ, 22 kΩ, 27 kΩ, 33 kΩ, 39 kΩ, 47 kΩ, 56 kΩ, 68 kΩ, 82 kΩ; 100 kΩ, 120 kΩ, 150 kΩ, 180 kΩ, 220 kΩ, 270 kΩ, 330 kΩ, 390 kΩ, 470 kΩ, 560 kΩ, 680 kΩ, 820 kΩ, and 1 MΩ.
* Available Capacitors- 1 μF, 2.2 μF, 3.3 μF, and 4.7 μF.
* BJT Model Provided –

\*MPS2222A MCE 1/26/96 \*Si 625mW 40V 600mA 300MHz pkg:TO-92 1,2,3 .MODEL QMPS2222A NPN (IS=.504F NF=1 BF=339 VAF=113 IKF=.36 ISE=1.63P NE=2 + BR=4 NR=1 VAR=24 IKR=.54 RE=.173 RB=.692 RC=69.2M XTB=1.5 + CJE=23.5P VJE=1.1 MJE=.5 CJC=10.6P VJC=.3 MJC=.3 TF=521P TR=272N)

# Implementation

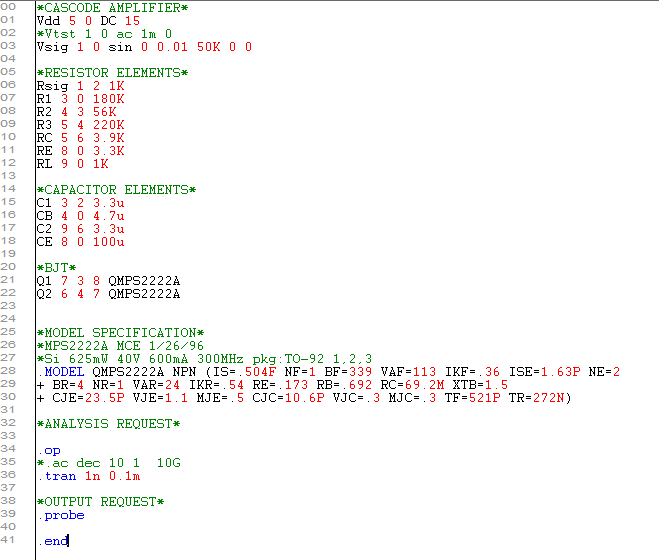
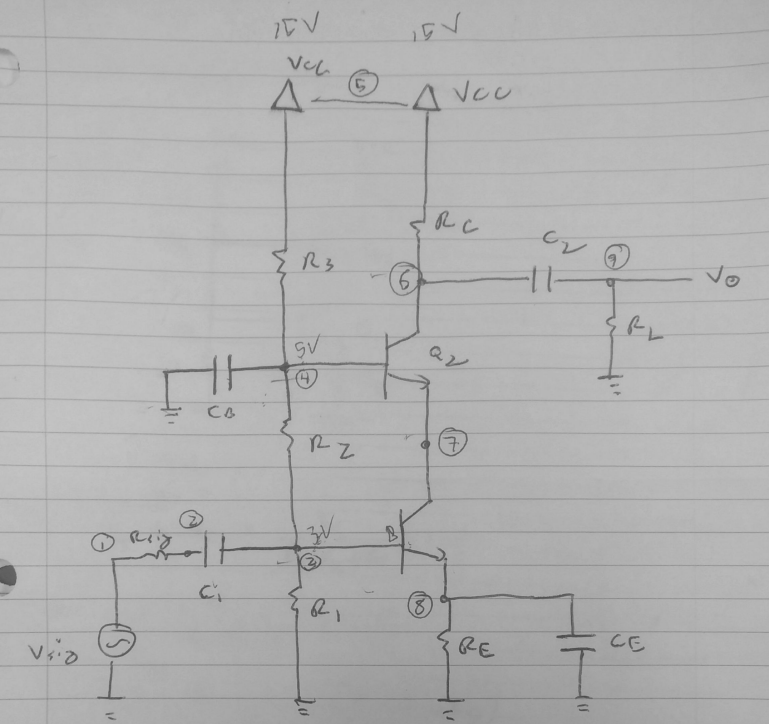


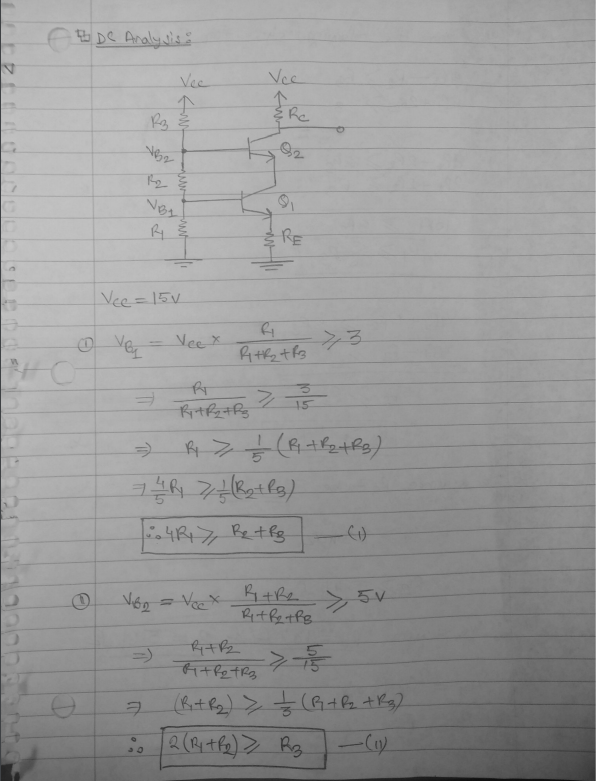
Figure : PSPICE implementation of Cascode Circuit

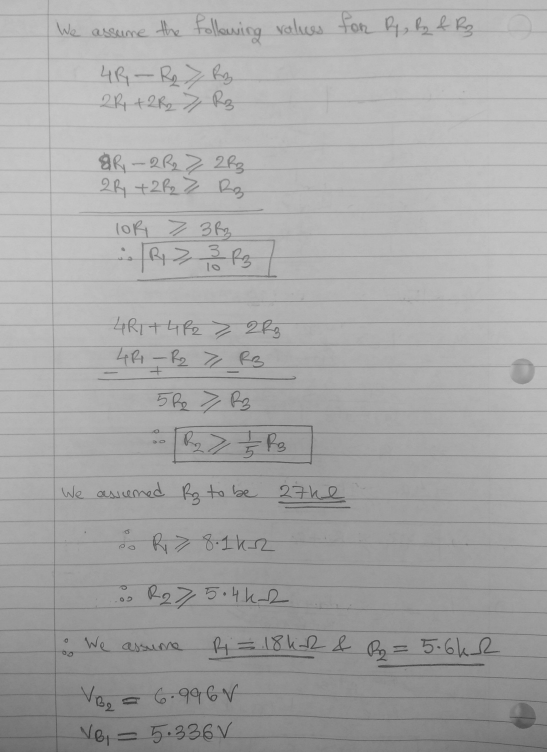
Two types of simulations were carried out, one AC and another Transient. The AC was used to determine the gain and the cutoff frequencies. The transient analysis gave us the values for the output voltage swing and DC power consumption. The input amplitude of the signals for both the simulations was set to 1mV. For DC it was set to 0.

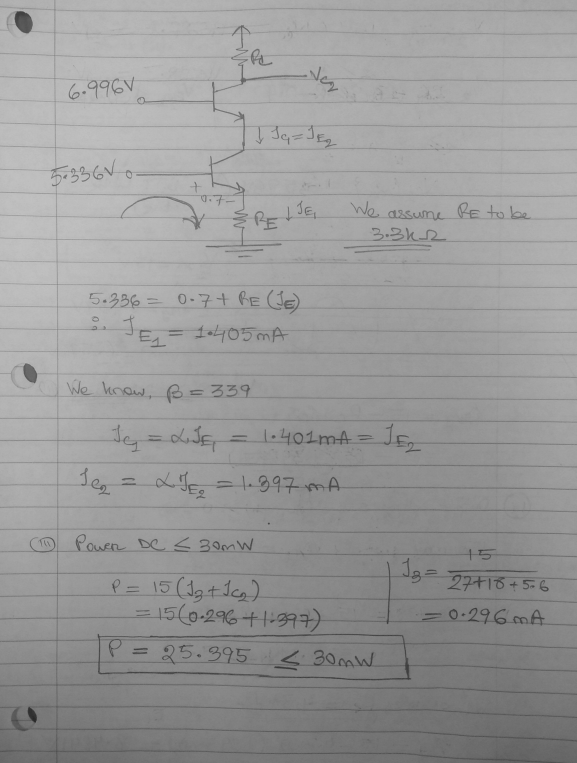
# Design Decisions and Optimization

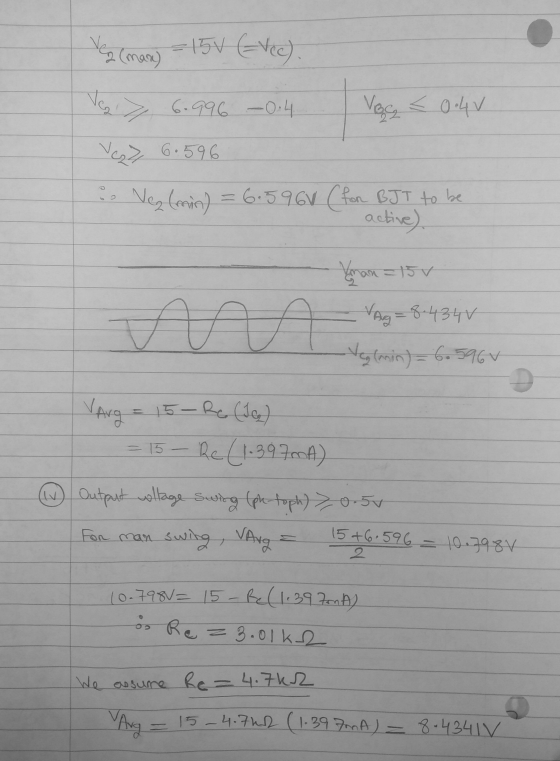
The following Diagrams show our design implementation calculated by hand –

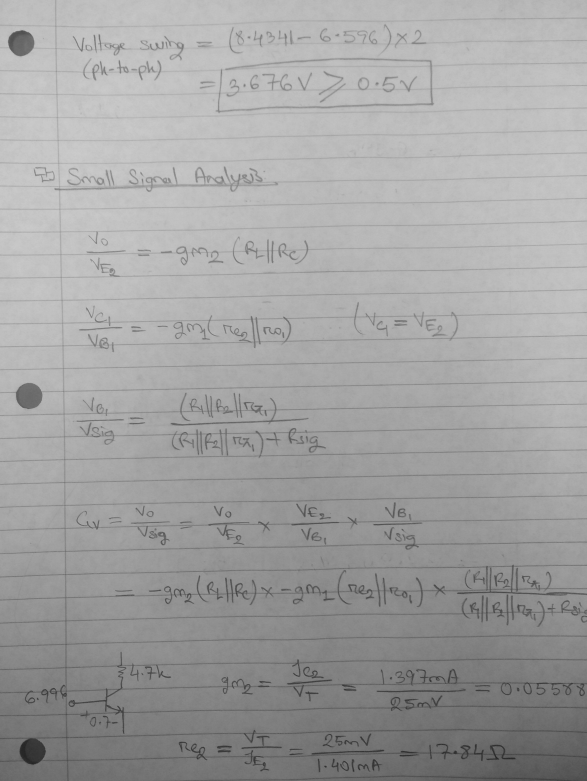


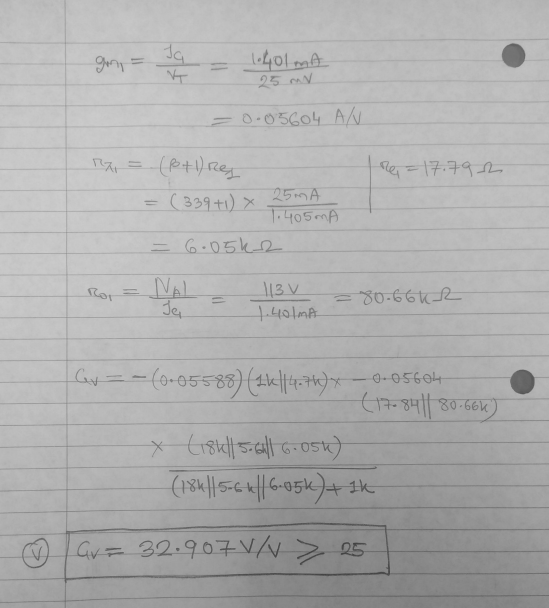


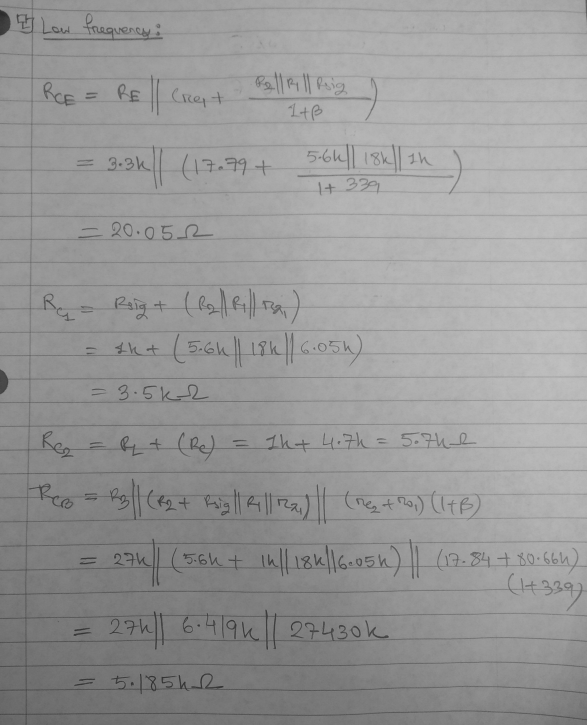


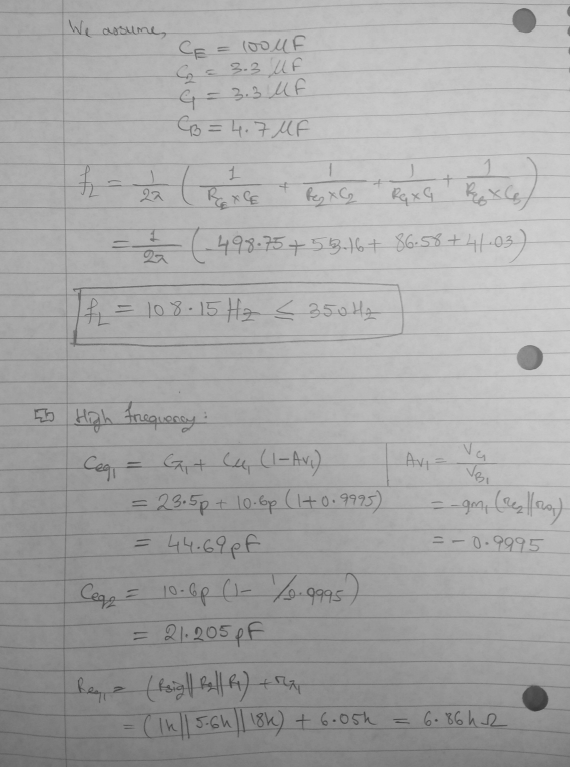


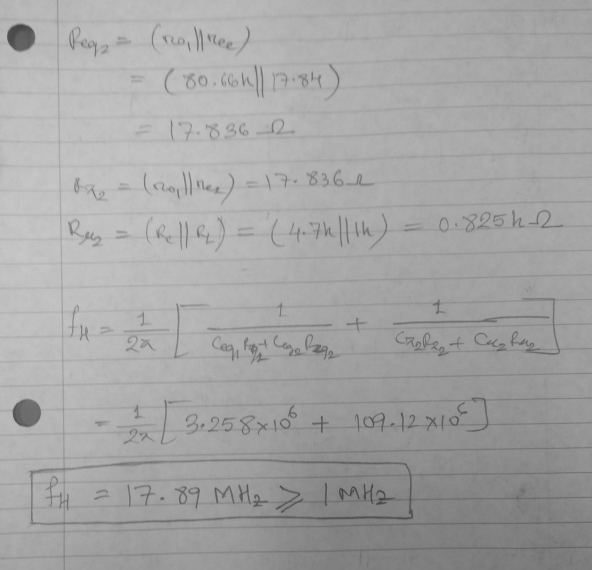












Values we ended up with are as follows. Note this is optimized by increasing resistance to decrease power consumption.

RSig 1K

R1 180K

R2 56K

R3 270K

RC 3.9K

RE 3.3K

RL 1K

C1 3.3u

CB 4.7u

C2 3.3u

CE 100u

# Observations and Testing

This section talks about the simulation results obtained and compared to the values that we calculated by ourselves.

## Meeting Requirements

The following outputs from our SPICE simulation shows the outputs for the requirements of our optimized design –

### Overall gain Gv (vo/vsig) ≥ 25 V/V

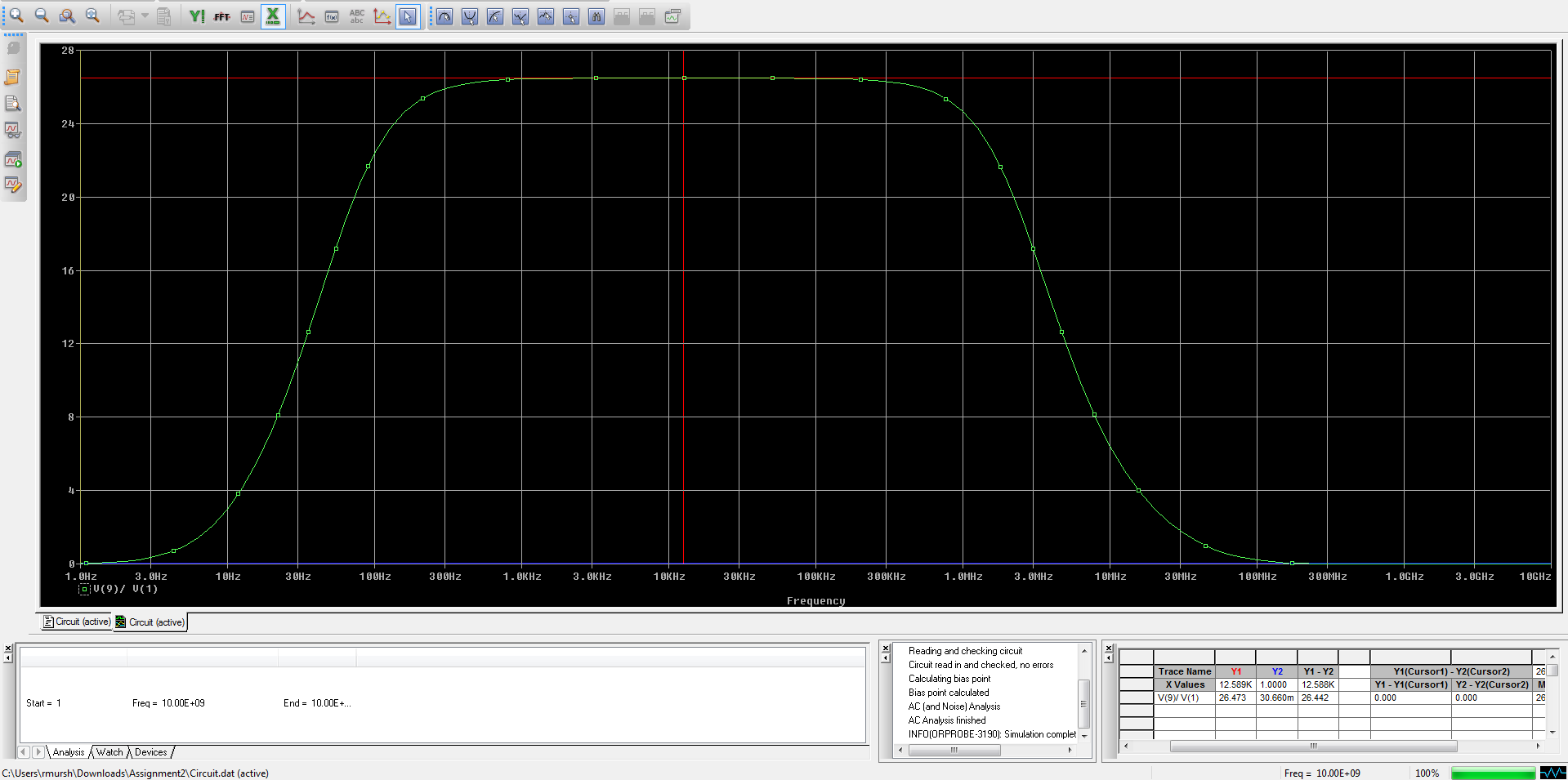


Figure : Gain of Cascode Amplifier

As it can be seen from the graph above our gain Vo/Vsig exceeds 25V/V.

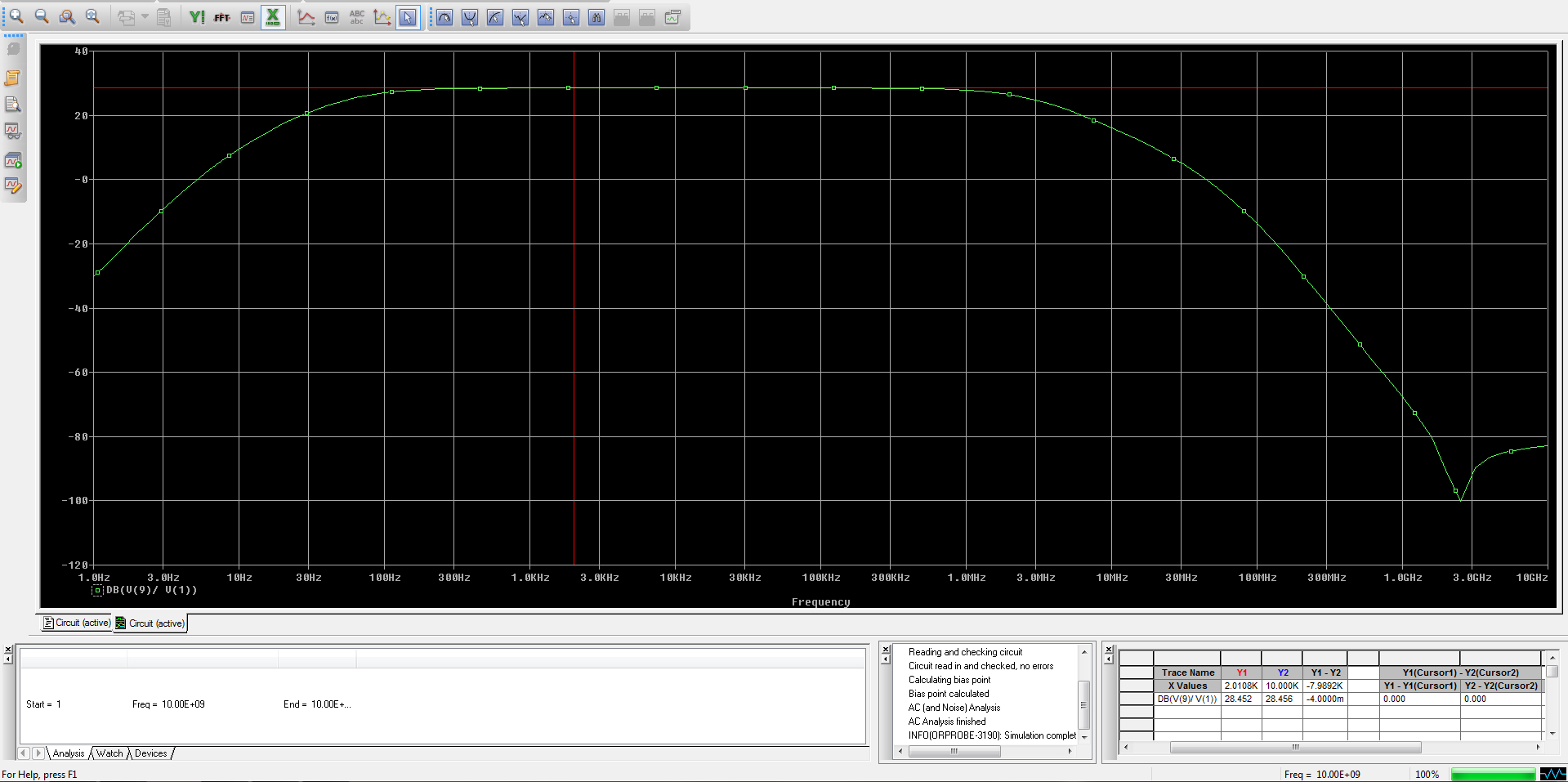


Figure : Gain in Decibels

### Bandwidth (3-dB frequencies) fL ≤ 350Hz, and fH ≥ 1 MHz

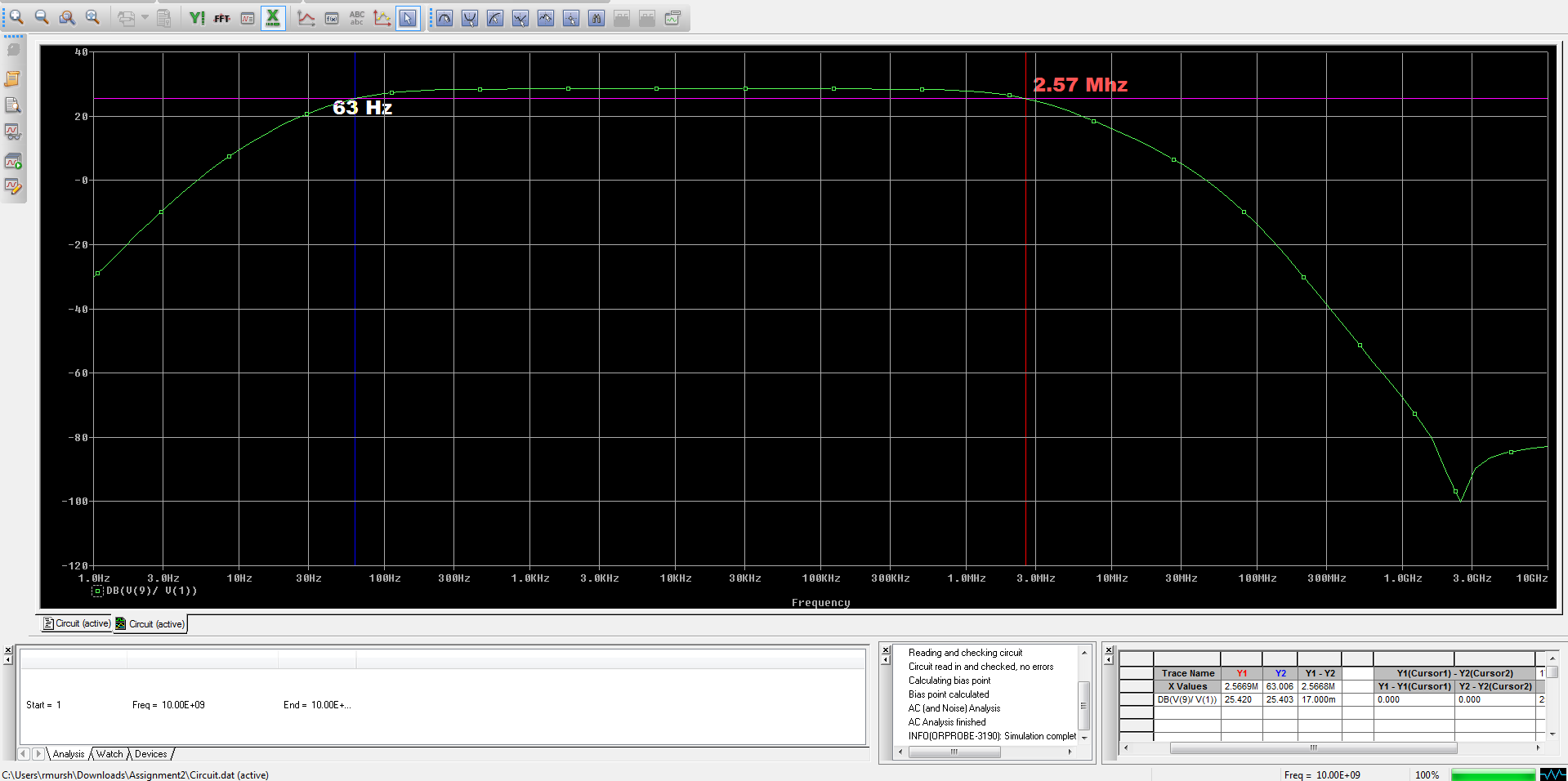


Figure : Low and high Cutoff Frequency

Low cutoff Frequency is around 71.3Hz which is less than 350Hz and High cutoff frequency is 2.57 Mhz

### Output voltage swing (peak-to-peak) ≥ 0.5 V

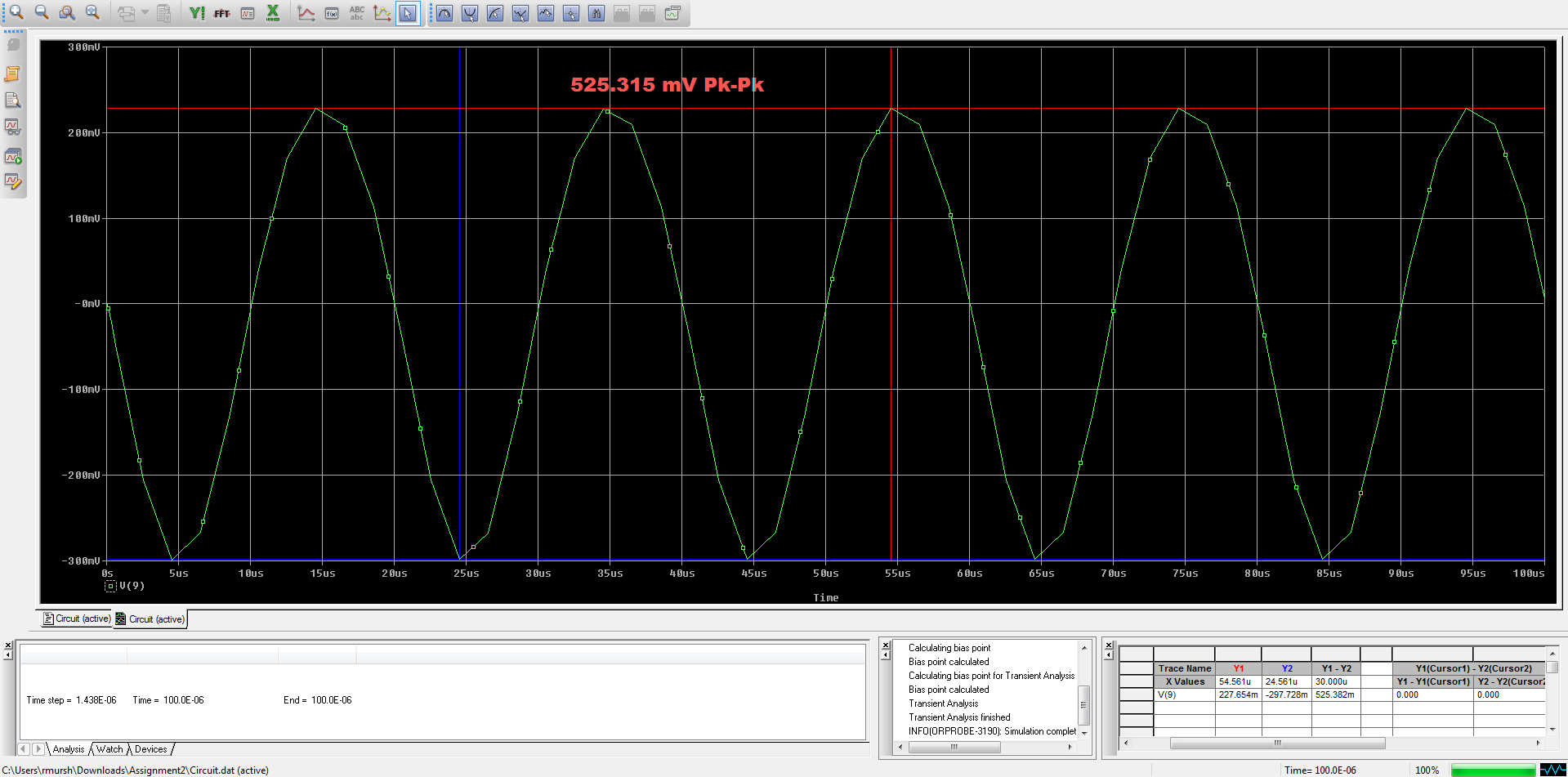


Figure : Output Voltage Swing

The output voltage swing for this amplifier is greater than 0.5V

### DC power consumption ≤ 30mW

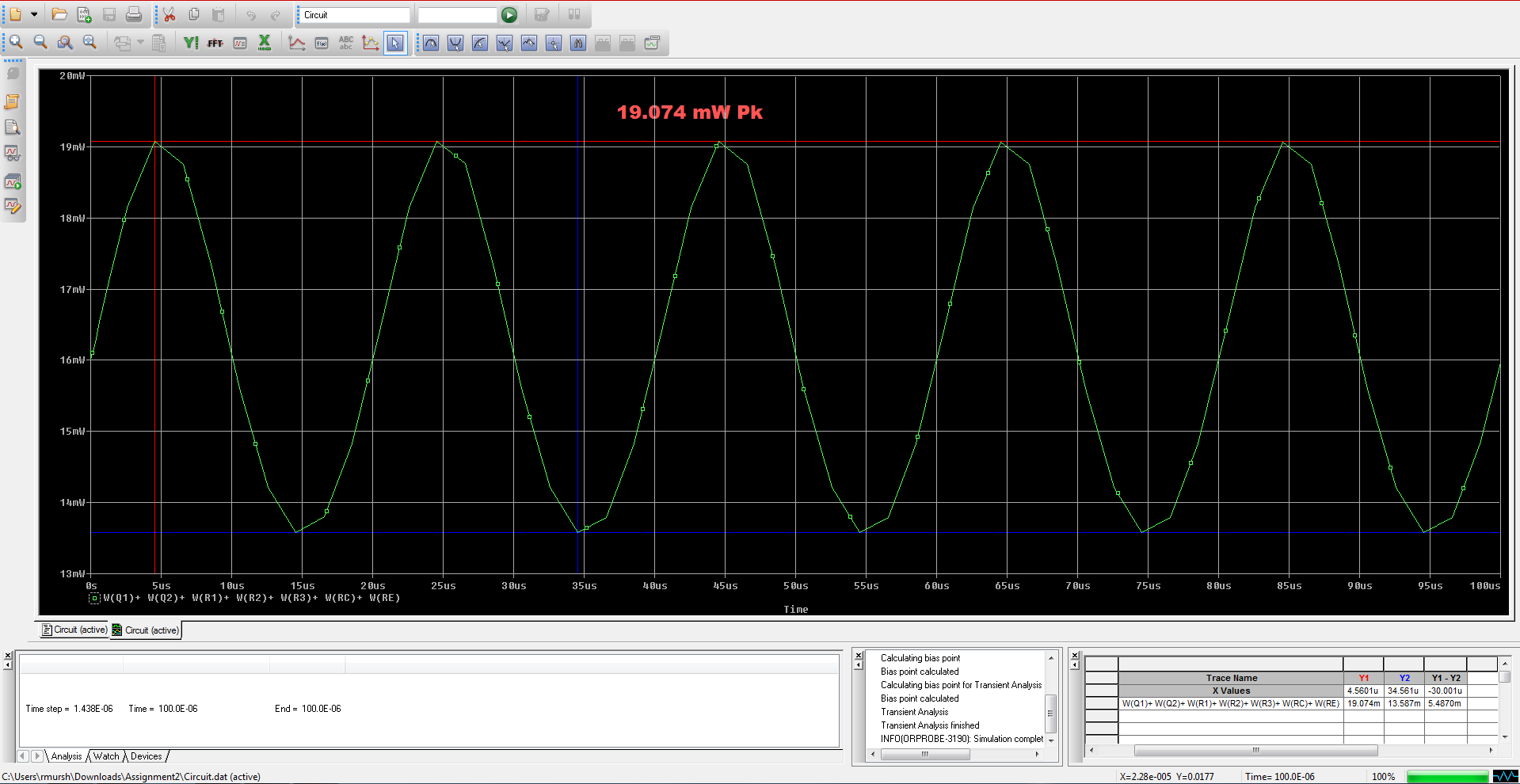


Figure : DC power consumption

The DC power consumed is less than 30V.

## Comparisons with Calculated Values

As per the specifications of the Assignment, the follows values were calculated and compared.

### Input Resistance

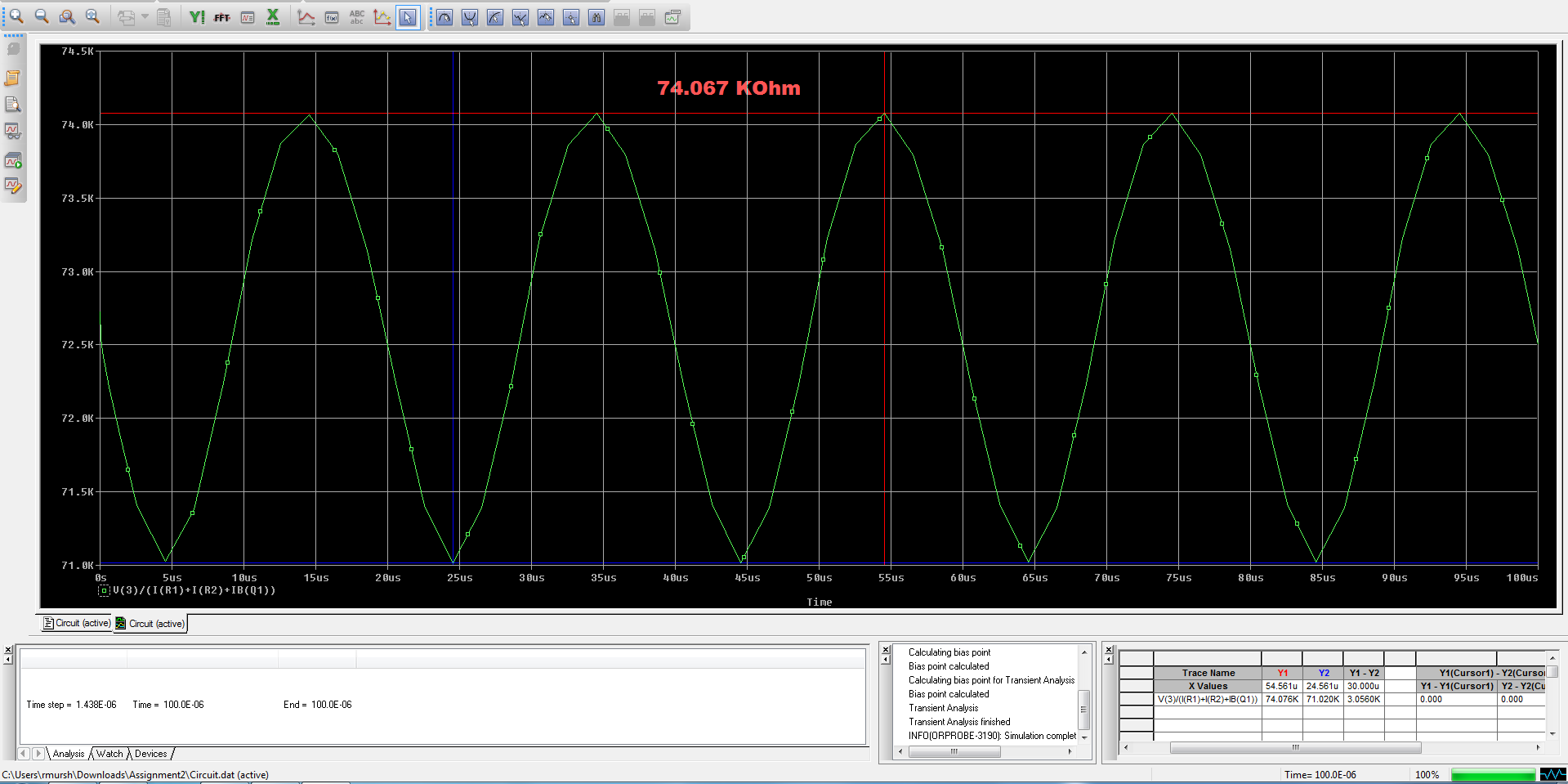


Figure : Rin for Amplifier

### Output Resistance

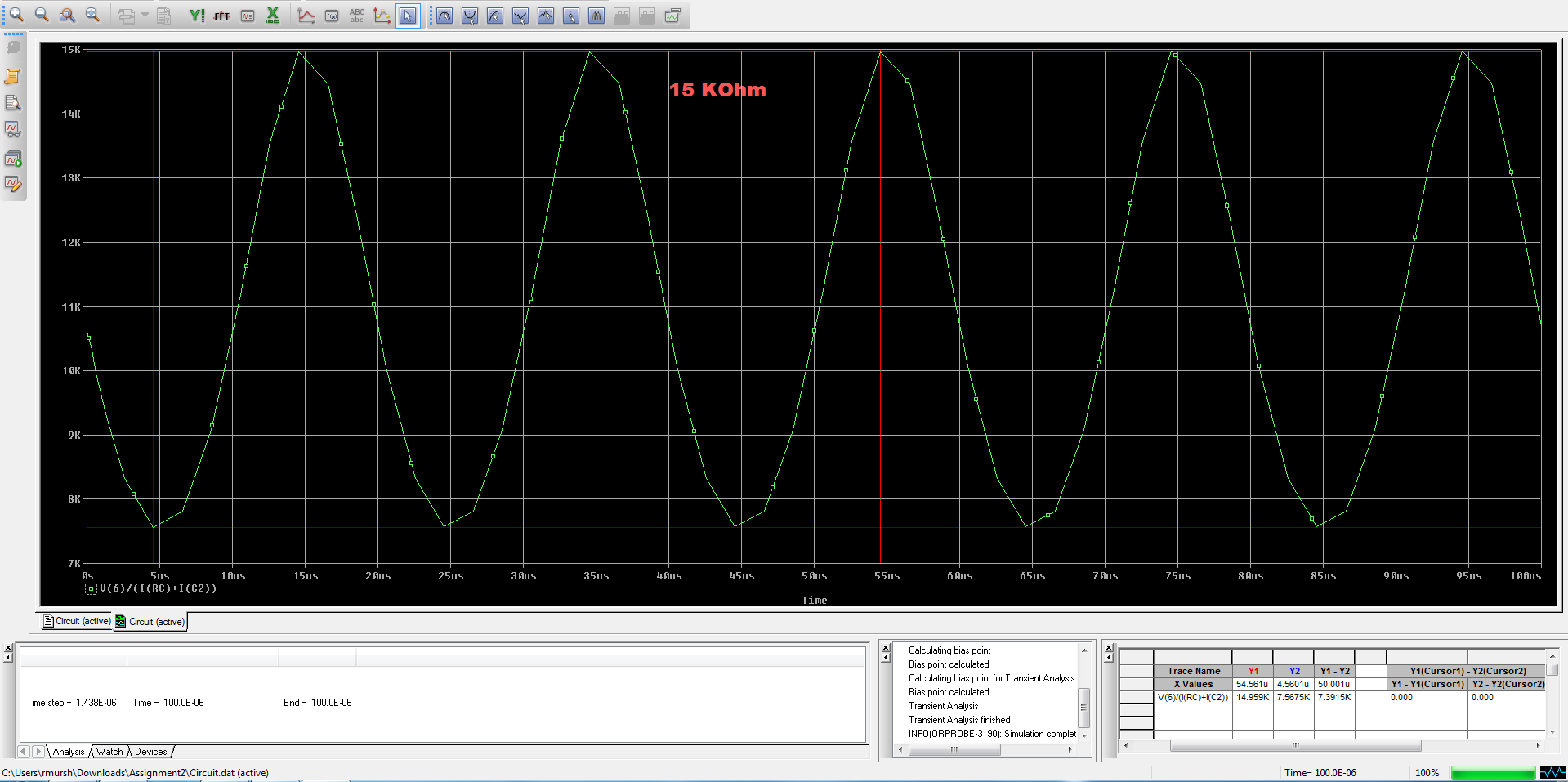


Figure : Output Resistance

### Voltage at Nodes

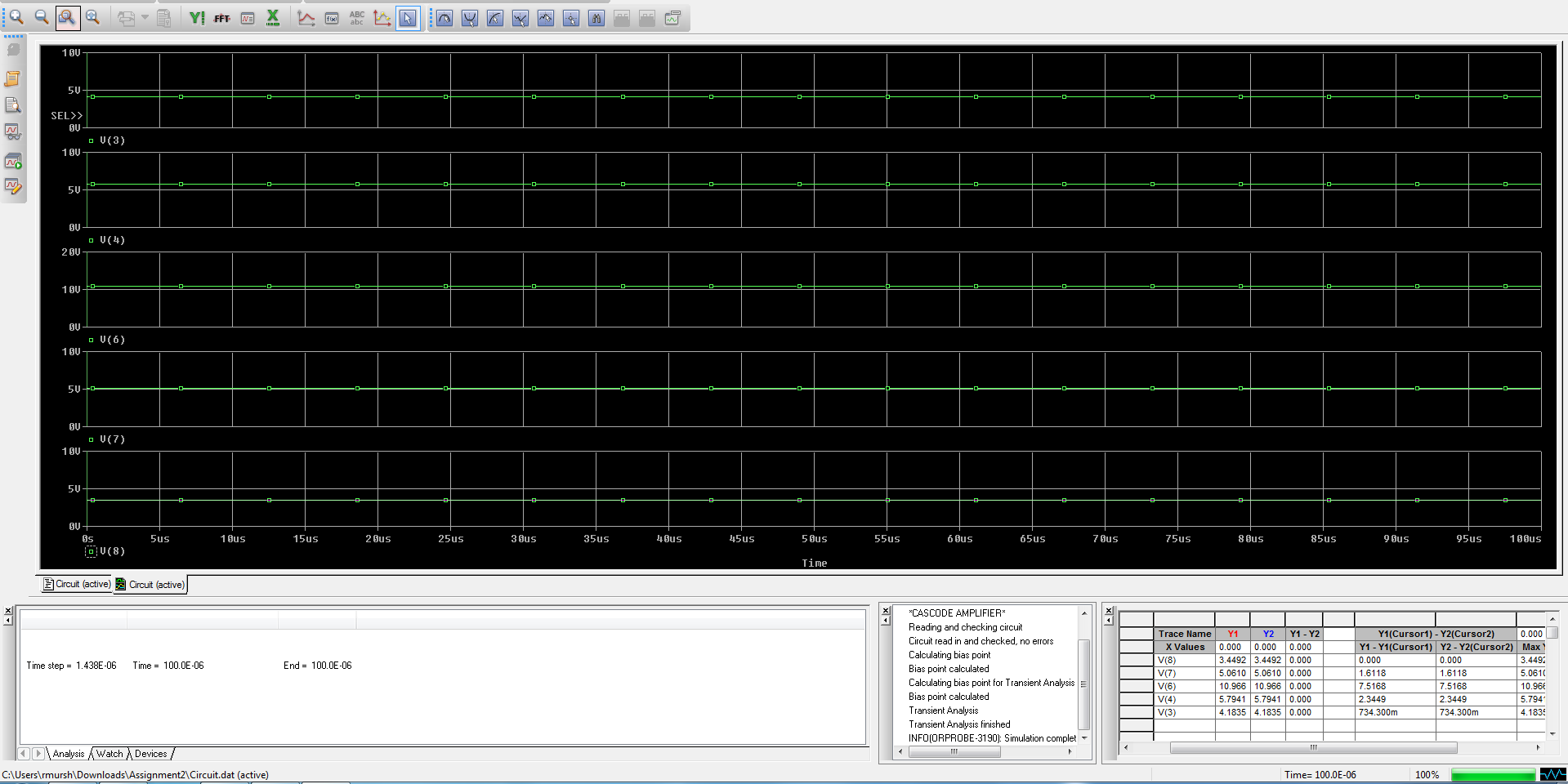


Figure : Voltages at Nodes

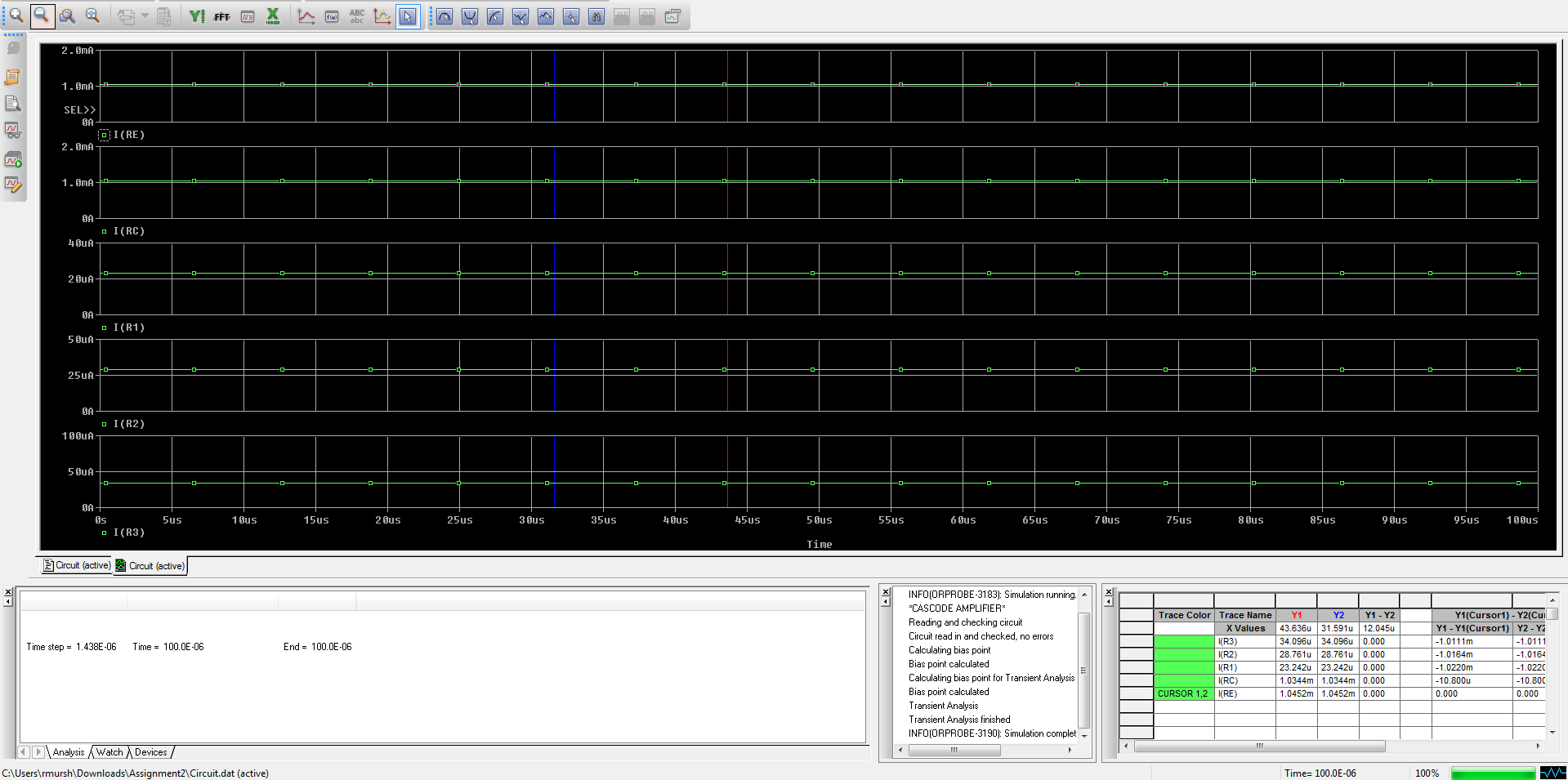


Figure : Currents through Elements

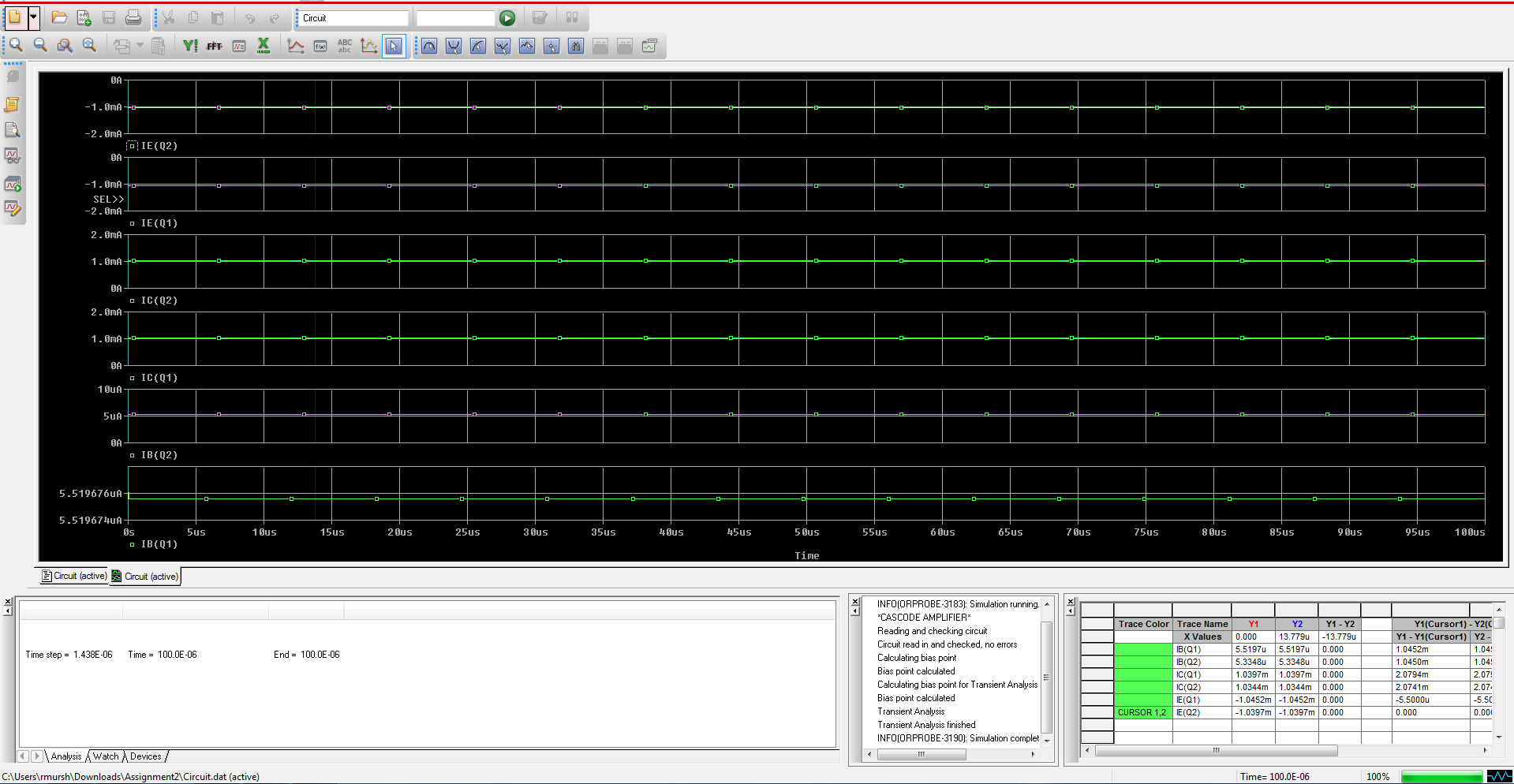
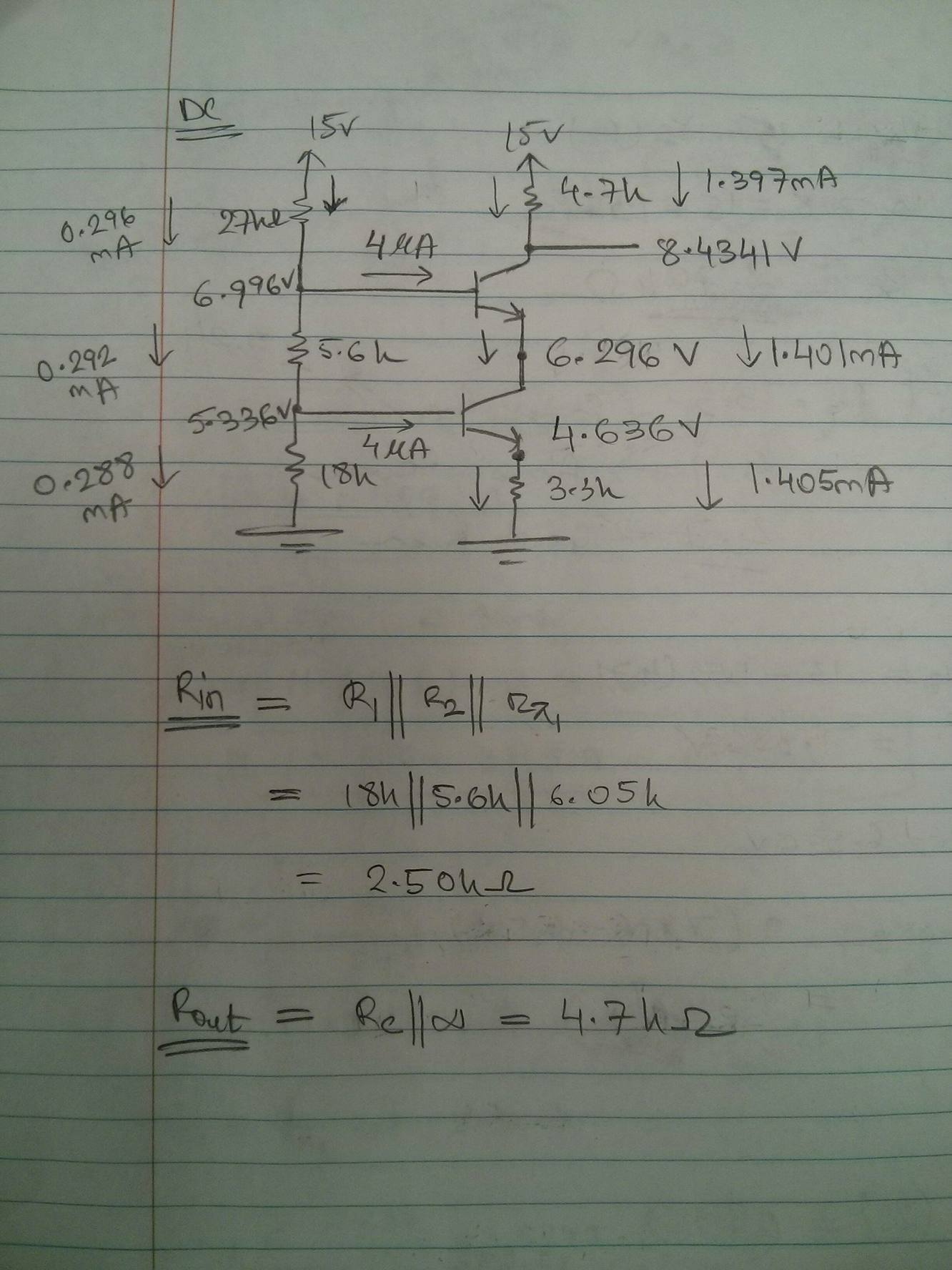


Figure : Currents passing through BJT Terminals

## Calculated Values

The values we found by hand are as follows –



# Conclusion

Our values ensured that all the requirements set by the design met. Moreover, we also managed to minimize the DC power consumption by the Elements in the circuit. The discrepancies in results may have occurred from assumptions about the model made during our calculations and the design in Spice.